Precision, 18-bit 8/4-Channel 200 kSPS SAR ADC

Features

- 18-bit resolution with no missing codes
- Throughput: 200 kSPS
- INL: ±1.5 LSB
- DNL: -0.6/+0.8 LSB
- Dynamic Range: 95 dB
- SNR: 94.5 dB
- THD: -105 dB
- Single-ended or Pseudo Differential Range: 0 V ~ V_{REF}
- Pseudo Differential Bipolar Range: ±V_{REF}/2
- No Pipeline Delay
- Single Supply: 4.75 V ~ 5.25 V
- Logic Interface: 1.8 V/2.5 V/3 V/5 V
- Package: QFN-20
- Operating Temperature Range: -40 °C to +85 °C

Applications

- Relay Protection
- Precision Data Acquisition
- Automated Testing
- Battery Test
- Optical Communication

General Description

The ZJC2103/5-18 is an 8/4-channel, 18-bit, SAR analog-to-digital converter (ADC). It operates up to 200 kSPS from a single power supply.

The ZJC2103/5-18 contains an 18-bit SAR ADC with no missing codes, an 8/4-channel, low crosstalk multiplexer to configure the inputs as single-ended, pseudo differential unipolar or bipolar; an internal low drift reference (selectable 2.5 V or 4.096 V) and reference driver; a temperature sensor; a selectable one-pole filter; and a digital sequencer which is useful for channels being continuously scanned in order.

The ZJC2103/5-18 uses a SPI interface for writing configuration register and receiving conversion codes. The digital interface uses a separate supply, VIO, which should be set to the host logic level.

ZJC2103/5-18 is available in 20-lead QFN packages. It is pin compatible with industry standard parts.

Block Diagram

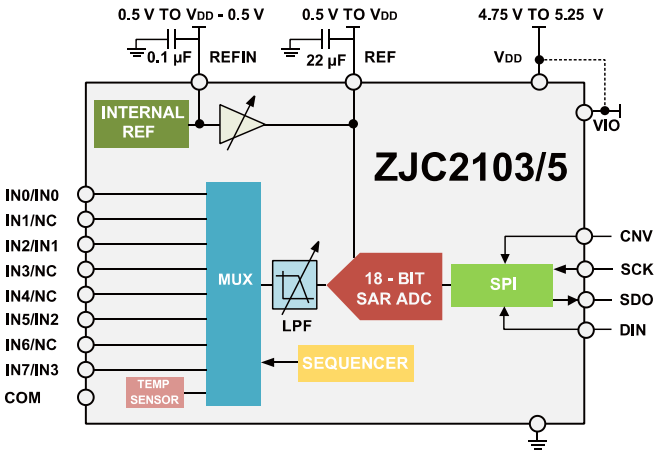


Figure 1. Block Diagram

Typical Characteristics

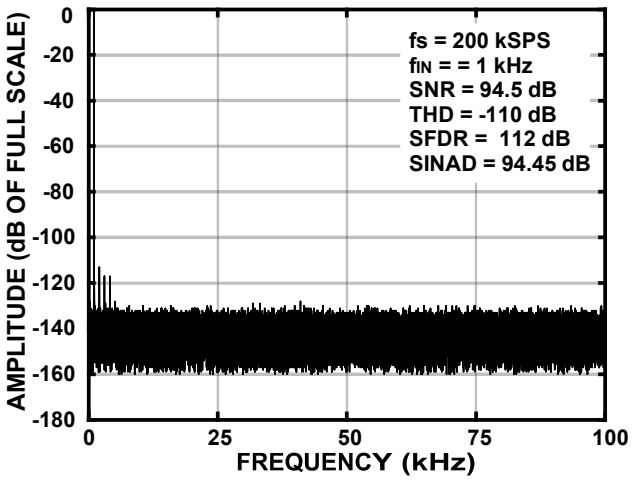


Figure 2. AC Characteristics

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Version (Release B) [1]

Revision History

Feb. 2025 - Release B

Updated Block Diagram, Figure 28, 31,32, 34, 35, 36, 37, Outline Dimensions, Ordering Guide, Product Order Model, Related Parts

Nov. 2023

Updated a few pictures and parameters

Aug. 2023 - Release A

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Pin Configurations and Function Descriptions

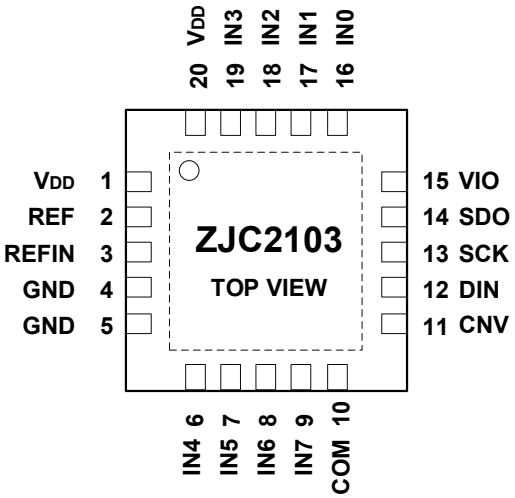


Figure 3. ZJC2103-18 Pin Configuration

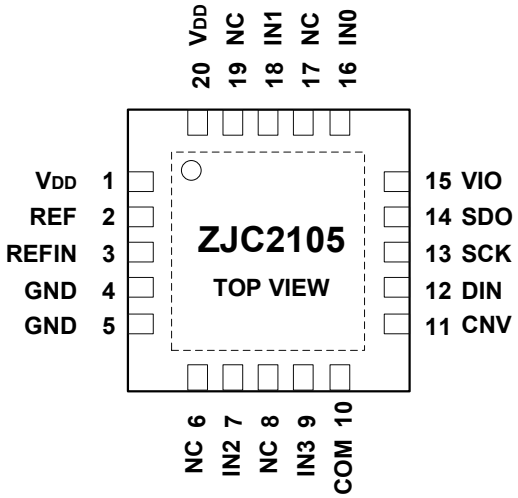


Figure 4. ZJC2105-18 Pin Configuration

Note: The exposed pad has no internal connection. Connect the pad to GND.

Mnemonic		Pin No.	Pin Type	Description
V_{DD}	V_{DD}	1, 20	Power Supply	Power Supply. Nominally 4.75 V to 5.5 V when using an external reference and decoupled with 10 µF and 100 nF capacitors.
REF	REF	2	Analog Input or Output	External Reference Input or Internal Reference Buffer Output. When the internal reference is enabled, it outputs a selectable reference 2.5 V or 4.096 V. When the internal reference is disabled and the buffer is enabled, REF produces a buffered reference voltage of the REFIN pin (4.096 V maximum). This pin needs decoupling with an external 10 or 22 µF capacitor close to REF pin. See the Reference Decoupling section.
REFIN	REFIN	3	Analog Input or Output	Internal Reference Output or External Reference Buffer Input. When using the internal reference, the internal un-buffered bandgap reference voltage is present. It needs decoupling with a 0.1 µF capacitor. When using the internal reference buffer, apply an external reference between 0.5 V and 4.096 V which is buffered to the REF pin.
GND	GND	4, 5	Ground	Power Supply Ground.
IN4	NC	6	Analog Input/NC	ZJC2103-18: Analog Input Channel 4. ZJC2105-18: No connection. Recommend connected to GND.
IN5	IN2	7	Analog Input	ZJC2103-18: Analog Input Channel 5. ZJC2105-18: Analog Input Channel 2.
IN6	NC	8	Analog Input/NC	ZJC2103-18: Analog Input Channel 6. ZJC2105-18: No connection. Recommend connected to GND.
IN7	IN3	9	Analog Input	ZJC2103-18: Analog Input Channel 7. ZJC2105-18: Analog Input Channel 3.

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Mnemonic		Pin No.	Pin Type	Description
COM	COM	10	Analog Input	Common Channel Input. All input channels, can be referenced to a common-mode point of 0 V or V_{REF} / 2.
CNV	CNV	11	Digital Input	Convert Input. On the rising edge, CNV initiates the conversion. During conversion, if CNV is high, the busy indictor is enabled.
DIN	DIN	12	Digital Input	Serial Data Input. This data input is used for writing to the 14-bit configuration register.
SCK	SCK	13	Digital Input	Serial Clock Input. This clock input is used to clock out the data on SDO and clock in data on DIN in an MSB first fashion.
SDO	SDO	14	Digital Output	Serial Data Output. The conversion codes are output on this pin by SCK. In unipolar modes, conversion codes are straight binary; in bipolar modes, conversion codes are twos complement.
VIO	VIO	15	Digital Power Supply	Digital Interface Power Supply. Nominally at the same supply as the host interface.
IN0	IN0	16	Analog Input	ZJC2103-18: Analog Input Channel 0. ZJC2105-18: Analog Input Channel 0.
IN1	NC	17	Analog Input	ZJC2103-18: Analog Input Channel 1. ZJC2105-18: No connection. Recommend connected to GND.
IN2	IN1	18	Analog Input	ZJC2103-18: Analog Input Channel 2. ZJC2105-18: Analog Input Channel 1.
IN3	NC	19	Analog Input	ZJC2103-18: Analog Input Channel 3. ZJC2105-18: No connection. Recommend connected to GND.
EPAD	EPAD	Exposed Pad	NC	The exposed pad is not connected internally. Recommended connecting the pad to the ground plane.

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Absolute Maximum Ratings [1]

Parameter	Rating
V_{DD}, REF, VIO to GND	-0.3 V ~ 6 V
REF, VIO to V_{DD}	-6 V ~ V_{DD} + 0.3 V
Analog Input Range (INx to GND)	-0.3 V ~ V_{DD} + 0.3 V
Digital Input to GND	-0.3 V ~ VIO + 0.3 V
Digital Output to GND	-0.3 V ~ VIO + 0.3 V
Storage Temperature Range	-65 °C to 150 °C
Junction Temperature Range	150 °C
Lead Temperature (Soldering, 10 seconds)	300 °C
Maximum Reflow Temperature [2]	260 °C
Electrostatic Discharge (ESD) [3]	
Human Body Model (HBM) [4]	1.5 kV
Charged Device Model (CDM) [5]	1 kV

Thermal Resistance [6]

Package	θ_{JA}	θ_{JC}	Unit
QFN-20	51	27	°C/W

[1] These ratings apply at 25 °C, unless otherwise noted. Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

[2] IPC/JEDECJ–STD-020 Compliant.

[3] Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

[4] ANSI/ESDA/JEDEC JS-001 Compliant.

[5] ANSI/ESDA/JEDEC JS-002 Compliant.

[6] θ_{JA} addresses the conditions for soldering devices onto circuit boards to achieve surface mount packaging.

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Specifications

The ● denotes the full temperature range for specified performance. Unless otherwise noted, V_{DD} = 4.75 V ~ 5.25 V, V_{REF} = V_{DD}, T_A = 25 °C.

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Resolution				18			
Input Characteristics							
Voltage Range		Unipolar	●	0		V_{REF}	V
		Bipolar	●	$-V_{REF}/2$		$+V_{REF}/2$	
Absolute input voltage		INx+ to GND	●	-0.1		V_{REF} + 0.1	V
		INx- or COM, Unipolar	●	-0.1		+0.1	V
		INx- or COM, Bipolar	●	$V_{REF}/2$ - 0.1		$V_{REF}/2$ + 0.1	V
Common Mode Rejection Ratio	CMRR	f_{IN} = 190 kHz			67		dB
Leakage Current		Acquisition Phase			1		nA
Input Impedance [1]							
Throughput							
Full Bandwidth		V_{DD} = 4.75 V to 5.25 V	●	0		200	kSPS
1/4 Bandwidth		V_{DD} = 4.75 V to 5.25 V	●	0		50	
Transient Response		Full - scale step	●			3150	ns
DC Accuracy							
No Missing Codes			●	18			bits
Integral Nonlinear Error	INL		●	-3	±1.5	+3	LSB [2]
Differential Nonlinear Error	DNL		●	-0.99	-0.6/+0.8	+1.5	LSB
Transition Noise		REF = V_{DD} = 5 V			1.5		LSB
Gain Error	GE	Single-ended	●	-40	±4	±40	LSB
Gain Error Matching					±4		LSB
Gain Error Temperature Drift					±0.5		ppm/°C
Zero Error	ZE	Single-ended	●	-20	±4	+20	LSB
Zero Error Matching					±2		LSB
Zero Error Temperature Drift					±0.3		ppm/°C
Power Supply Sensitivity		V_{DD} = 5 V ± 5%			±2		LSB

1 See the Analog Inputs section.
2 LSB means least significant bit. 1 LSB = 19.1 μV for 5 V input range.

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Parameter	Symbol	Conditions		Min	Typ	Max	Unit
AC Accuracy							
Dynamic Range	DR	V_{REF} = 5 V	●	94	95		dB [3]
SNR	SNR	f_{IN} = 1 kHz, V_{REF} = 5 V	●	93	94.5		dB
		f_{IN} = 1 kHz, V_{REF} = 4.096 V, internal ref	●	90.5	92.5		
		f_{IN} = 1 kHz, V_{REF} = 2.5 V, internal ref	●	86.5	88.5		
Signal-to (Noise + Distortion)	SINAD	f_{IN} = 1 kHz, V_{REF} = 5 V	●	92.9	94.4		dB
		f_{IN} = 1 kHz, V_{REF} = 4.096 V, internal ref	●	90.3	92.3		
		f_{IN} = 1 kHz, V_{REF} = 2.5 V, internal ref	●	86.4	88.4		
Spurious-Free Dynamic	SFDR	f_{IN} = 1 kHz, V_{REF} = 5 V			106		dB
Total Harmonic Distortion	THD	f_{IN} = 1 kHz, V_{REF} = 5 V			-105		dB
Channel Crosstalk		f_{IN} = 1 kHz, V_{REF} = 5 V			-120		dB
External Reference Input							
Voltage Range		REF Input	●	0.5		V_{DD} + 0.3	V
		REFIN Input (Buffer Enabled)	●	0.5		V_{DD} - 0.5	
Load Current		Sinewave Input			50		μA
Internal Reference Output							
REF Output Voltage		4.096 V, @ 25 °C	●	4.092	4.096	4.100	V
		2.5 V, @ 25 °C	●	2.495	2.5	2.505	
REFIN Output Voltage		REF = 4.096 V, @ 25 °C			2.42		V
		REF = 2.5 V, @ 25 °C			1.21		
REF Output Current					300		μA
Temperature Drift	T_c	-40 °C to +85 °C	●		6	10	ppm/°C
		0 °C to +85 °C			2		ppm/°C
Line Regulation		V_{DD} = 5 V ± 5%			20		ppm/V
Turn-On Settling Time		C_{REFIN} = 0.1 μF, C_{REF} = 10 μF			10		ms
Sampling Dynamics							
-3 dB Analog Input Bandwidth		V_{DD} = 5 V, Full Bandwidth			6		MHz
		V_{DD} = 5 V, 1/4 Bandwidth			1.5		
Aperture Delay		V_{DD} = 5 V			3		ns

[3] Unless otherwise noted, all specifications expressed in decibels (dB) are referenced to full-scale input FSR and are tested with an input signal 0.5 dB below full-scale.

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Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Temperature Sensor							
Output Voltage		@ 25 °C			300		mV
Temperature Sensitivity					1		mV/°C
Digital Input							
Logic Level	V_{IL}		●	-0.3		0.3 x VIO	V
	V_{IH}		●	0.7 x VIO		VIO+0.3	
Input Current	I_{IL}		●	-1		+1	µA
	I_{IH}		●	-1		+1	
Digital Output							
Data Format		Single-ended, or Pseudo Diff Unipolar		Serial 18-bit, straight binary			
		Pseudo Diff Bipolar		Serial 18-bit, twos complete			
Logic Low Voltage	V_{OL}	I_{OUT} = +200 µA	●			0.4	V
Logic High Voltage	V_{OH}	I_{OUT} = -200 µA	●	VIO - 0.3			V
Power Supplies							
V_{DD}		Specified performance		4.75		5.25	V
VIO		Specified performance		1.8		V_{DD} + 0.3	V
Power-down Current [4,5]		V_{DD} and VIO = 5 V, @ 25 °C			50		nA
Power Consumption		V_{DD} = 5 V, 1 kSPS	●		35	39	µW
		V_{DD} = 5 V, 100 kSPS	●		3.5	3.9	mW
		V_{DD} = 5 V, 200 kSPS	●		7.1	7.9	mW
		V_{DD} = 5 V, 200 kSPS, internal ref	●		11.5	12.9	mW
Temperature Range							
Specified Performance		T_{MIN} to T_{MAX}		-40		+85	°C

4 In the acquisition phase.
5 All digital inputs are forced to VIO or GND as required.

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Timing Specifications

The ● denotes the full temperature range for specified performance. Unless otherwise specified, V_{DD} = 4.75 V ~ 5.25 V, V_{REF} = V_{DD}, VIO = 1.8 V ~ V_{DD}, T_A = 25 °C.

Parameter	Symbol		Min	Typ	Max	Unit
Conversion Time: CNV Rising Edge to Data Available	t_{CONV}	●			1.85	μs
Acquisition Time	t_{ACQ}	●	0.65			μs
Time Between Conversions	t_{CYC}	●	2.5			μs
Data Write / Read During Conversion	t_{DATA}	●			1.0	μs
CNV Pulse Width	t_{CNVH}	●	10			ns
SCK Period (VIO > 3.3 V)	t_{SCK}	●	15			ns
VIO above 2.7 V		●	20			ns
VIO above 2.3 V		●	25			ns
VIO above 1.8 V		●	40			ns
SCK Low Time (VIO > 3.3 V)	t_{SCKL}	●	7.5			ns
SCK High Time (VIO > 3.3 V)	t_{SCKH}	●	7.5			ns
SCK Falling Edge to Data Remain Valid	t_{HSDO}	●	4			ns
SCK Falling Edge to Data Valid Delay	t_{DSDO}					
VIO above 2.7 V		●			17	ns
VIO above 2.3 V		●			18	ns
VIO above 1.8 V		●			21	ns
CNV Low to SDO MSB Valid	t_{EN}					
VIO above 2.7 V		●			22	ns
VIO above 2.3 V		●			25	ns
VIO above 1.8 V		●			28	ns
CNV High or Last SCK Falling Edge to SDO High Impedance	t_{DIS}				25	ns
CNV Low to SCK Rising Edge	t_{CLCLK}	●	10			ns
Last SCLK Falling Edge to CNV Rising Edge Delay	t_{QUIET}	●	140			ns
DIN Valid Setup Time from SCK Rising Edge	t_{SDIN}	●	5			ns
DIN Valid Hold Time from SCK Rising Edge	t_{HDIN}	●	5			ns

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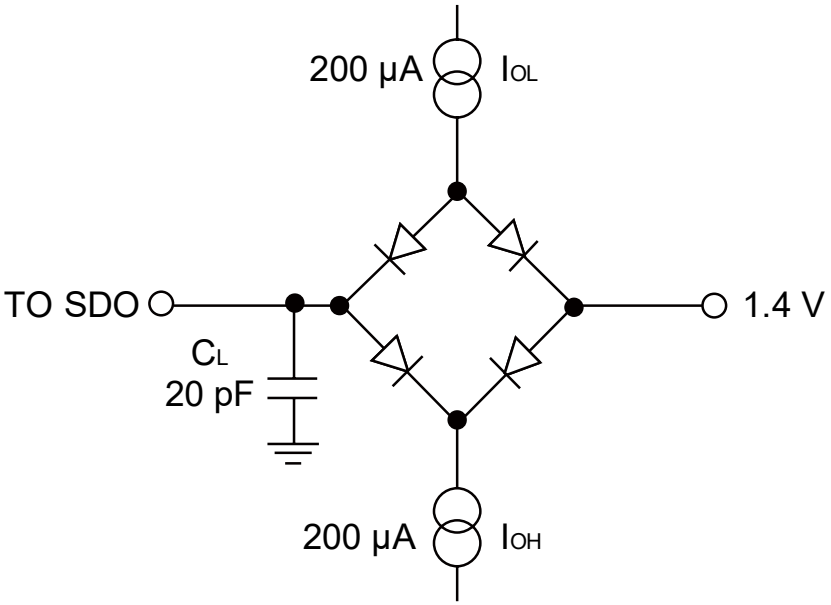


Figure 5. Load Circuit for Digital Interface Timing

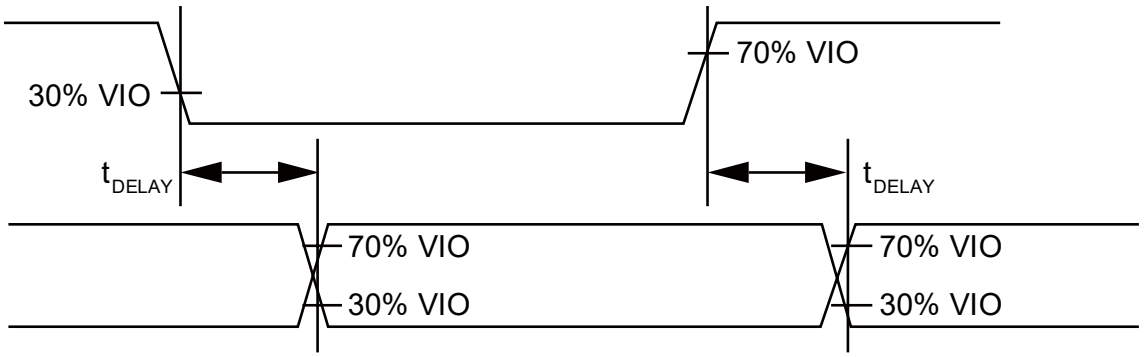


Figure 6. Voltage Levels for Timing

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Typical Performance Characteristics

Unless otherwise noted, V_{DD} = 5.0 V, REF = 5.0 V, VIO = 3.3 V, T_A = 25 °C.

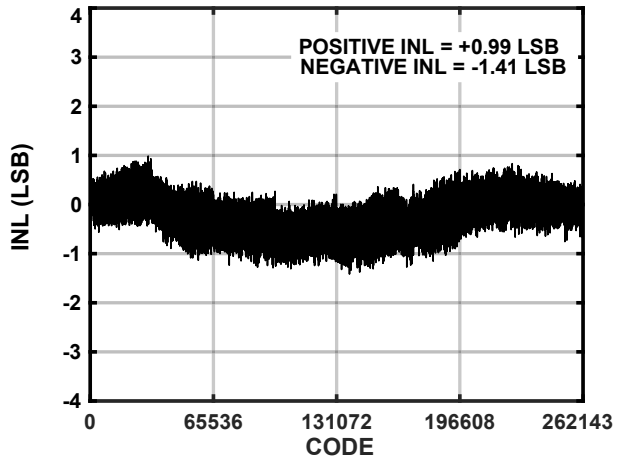


Figure 7. Integral Nonlinearity vs. Code

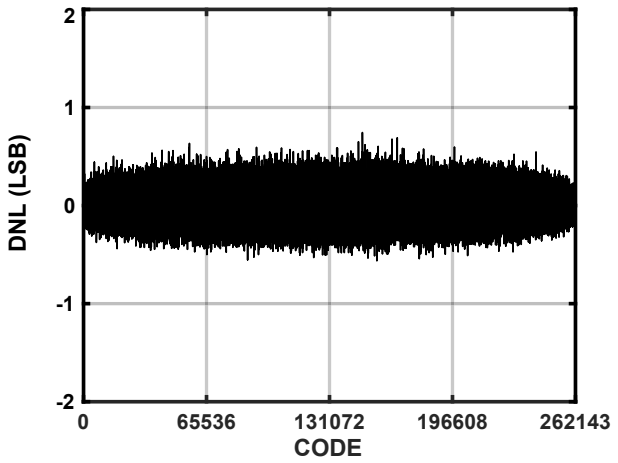


Figure 8. Differential Nonlinearity vs. Code

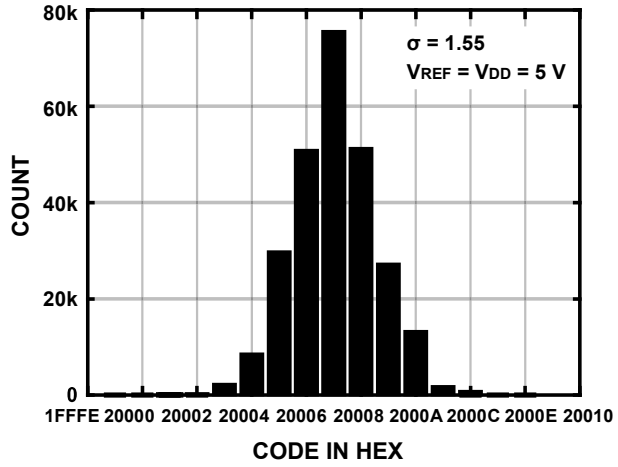


Figure 9. Histogram of DC Input (Code Center)

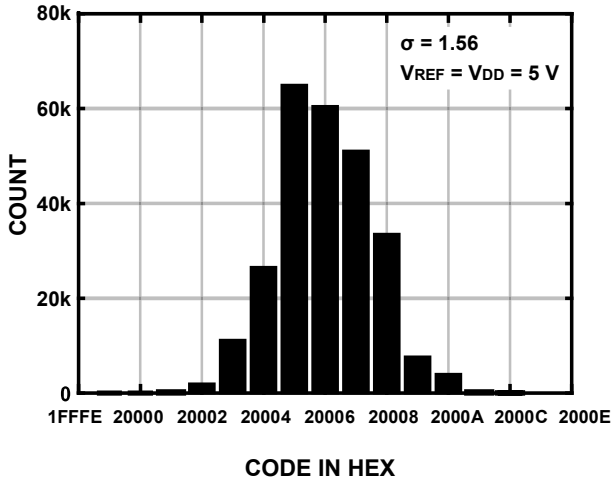


Figure 10. Histogram of DC Input (Code Transition)

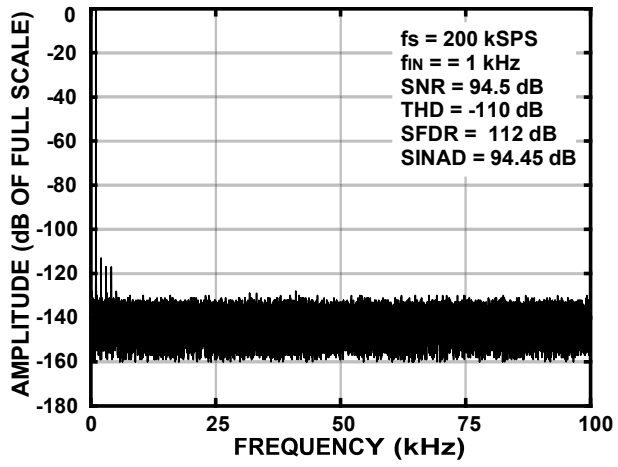


Figure 11. FFT Plot V_{REF} = V_{DD} = 5 V

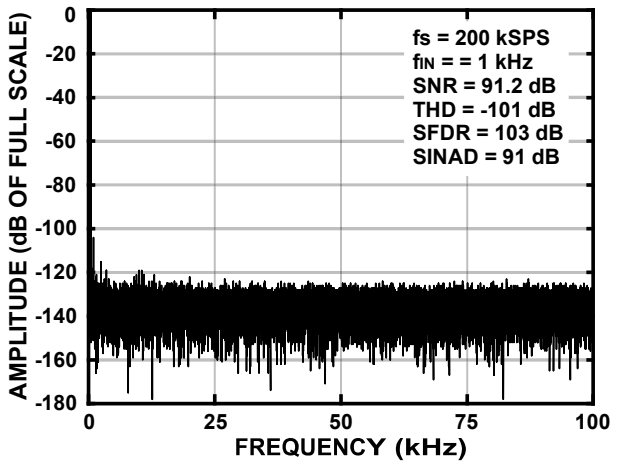


Figure 12. FFT Plot Internal V_{REF} = 4.096 V

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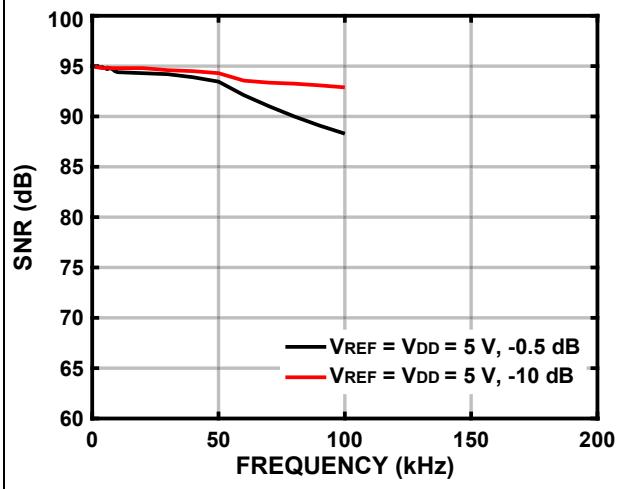


Figure 13. SNR vs Frequency

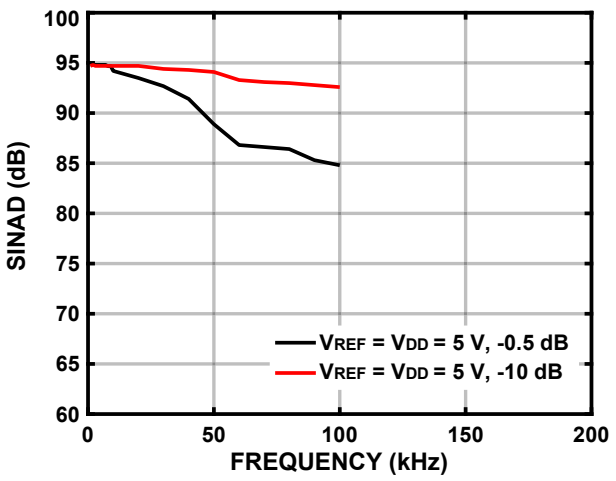


Figure 14. SINAD vs Frequency

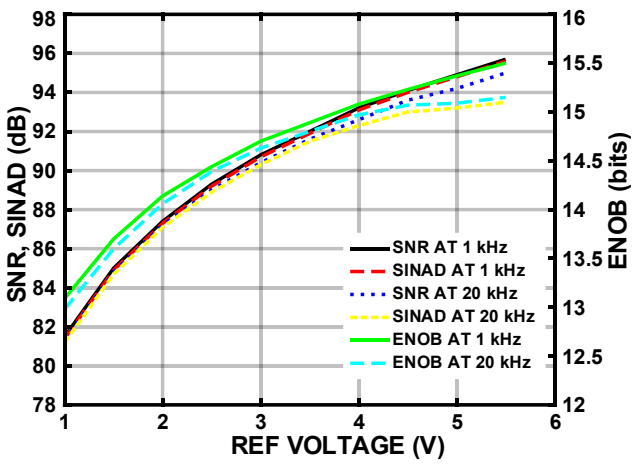


Figure 15. SNR, SINAD and ENOB vs. Reference Voltage

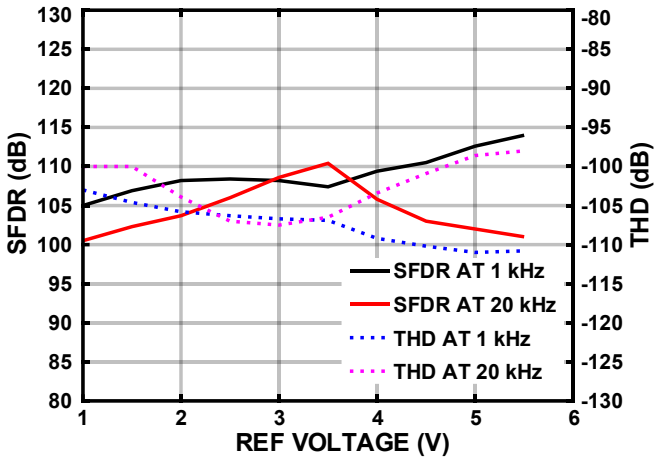


Figure 16. THD, SFDR vs. Reference Voltage

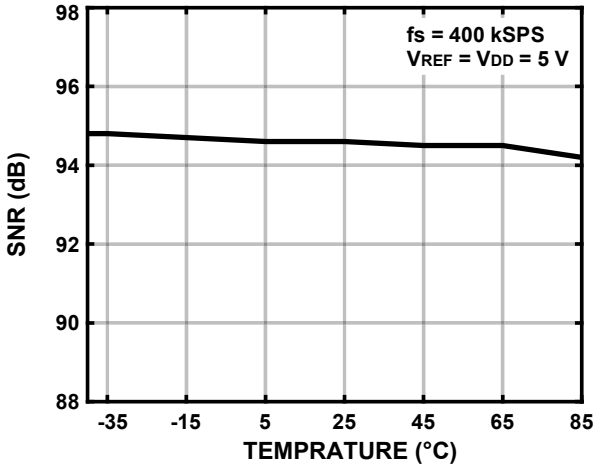


Figure 17. SNR vs. Temperature

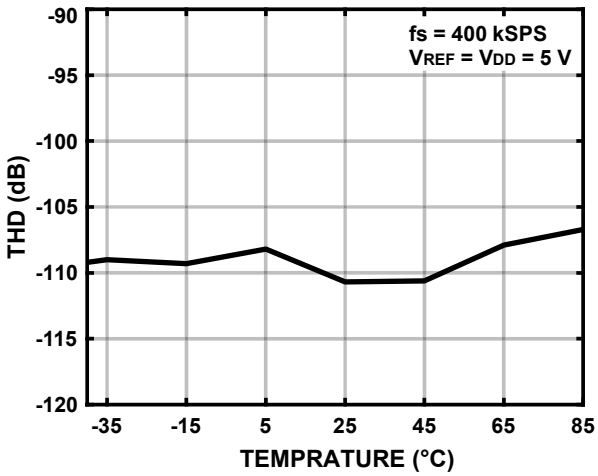


Figure 18. THD vs. Temperature

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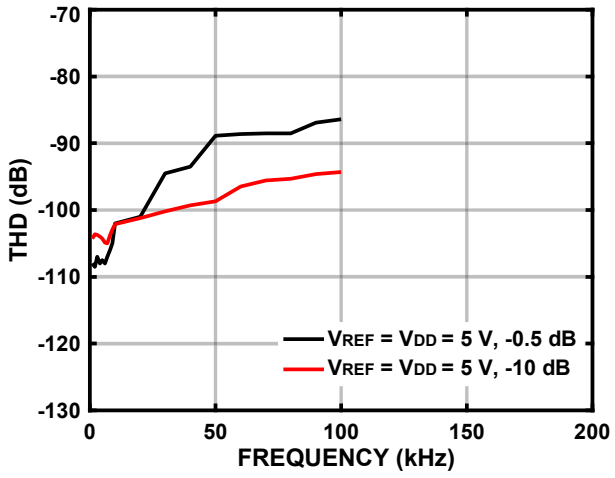


Figure 19. THD vs. Frequency

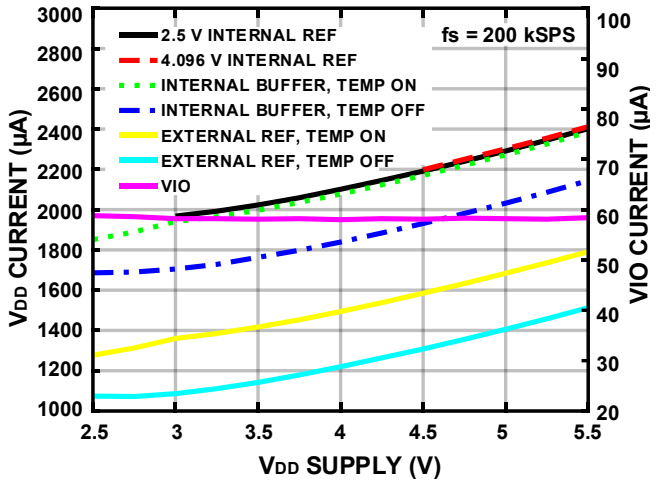


Figure 20. V_{DD} and VIO Current vs. V_{DD} Supply

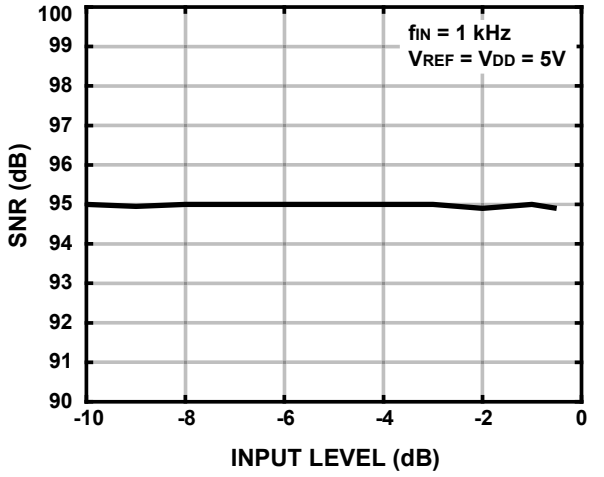


Figure 21. SNR vs. Input Voltage

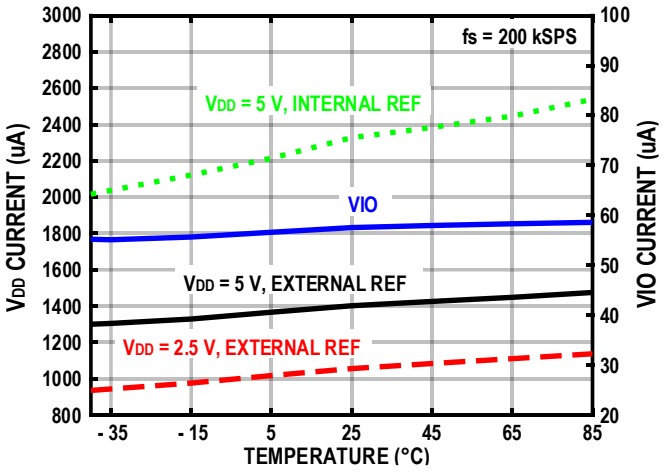


Figure 22. V_{DD} and VIO Current vs. Temperature

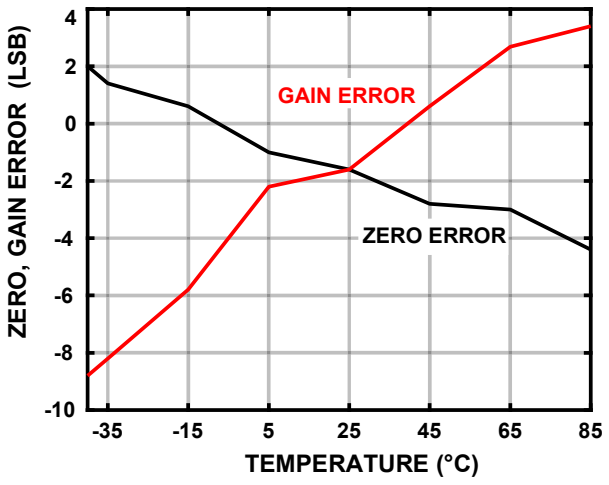


Figure 23. Zero Input, Gain Error vs. Temperature

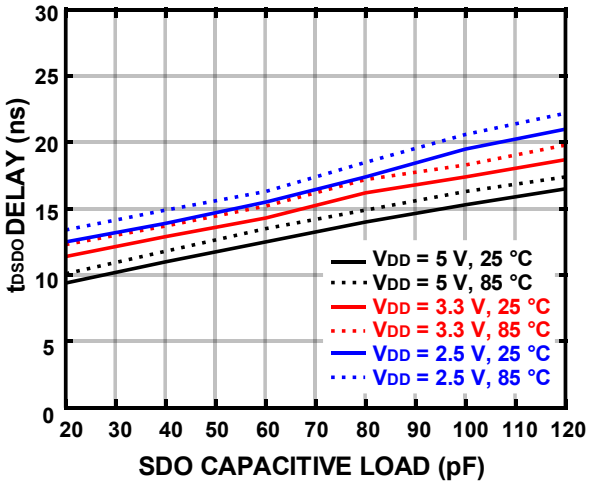


Figure 24. t_{DSDO} Delay vs Capacity Load and Voltage

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Theory of Operation

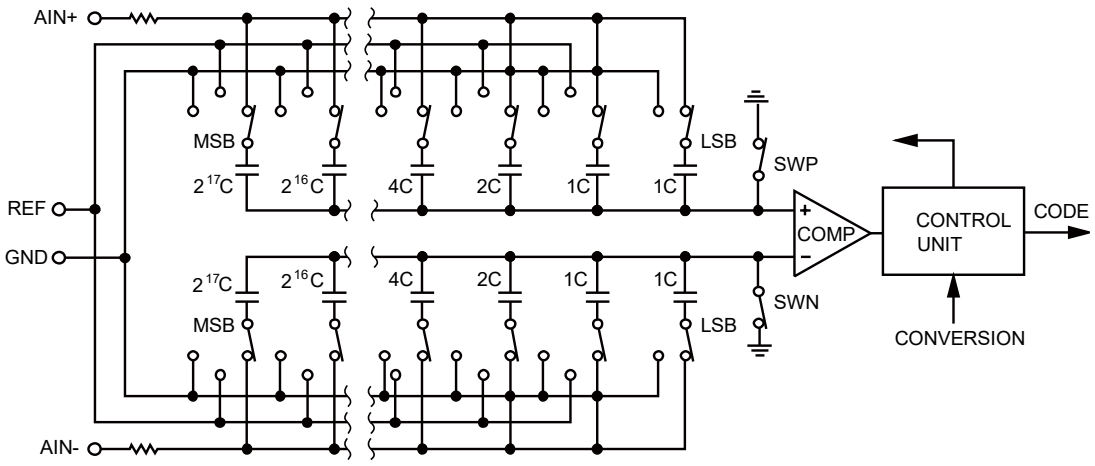


Figure 25. ADC Simplified Circuit Diagram

Circuit Structure

The ZJC2103/5-18 is an 8/4-channel, 18-bit, charge redistribution successive approximation register analog-to-digital converter. The ZJC2103/5-18 is capable of running up to 200 kSPS and powers down between conversions.

The ZJC2103/5-18 contains an 18-bit SAR ADC, an 8/4-channel, low crosstalk multiplexer to configure the inputs as single-ended, pseudo differential unipolar or bipolar; an internal low drift reference (selectable 2.5 V or 4.096 V) and reference driver; a temperature sensor; a selectable one-pole filter; and a digital sequencer which is useful for channels being continuously scanned in order.

Convertor Operation

Figure 25 is a simplified circuit diagram of ZJC2103/5-18.

In the acquisition phase, the array node connected to the input of the comparator is short connect to GND via the SW+ and SW-. All individual switches are connected to analog inputs. When the acquisition phase is complete and a rising edge occurs on the CNV input, the conversion phase is initiated. When the conversion phase begins, the SW+ and SW- disconnect first. The two capacitor arrays are then disconnected from the input and connected to the GND input. By switching the elements of the capacitor array between GND and REF, the comparator input will vary in binary weighted voltage steps ($V_{REF}/2^1$, $V_{REF}/2^2$, ..., $V_{REF}/2^{18}$). The control logic toggles these switches in sequence starting with the MSB, and the comparator is brought back into balance each time. After this phase is complete, the device returns to the acquisition phase, and the control logic generates the ADC output code.

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Transfer Function

When configured as singled-ended or pseudo differential unipolar (single-ended INx to GND, COM to GND, temperature sensor, IN- to GND), the code is straight binary. The ideal transfer characteristic is shown below:

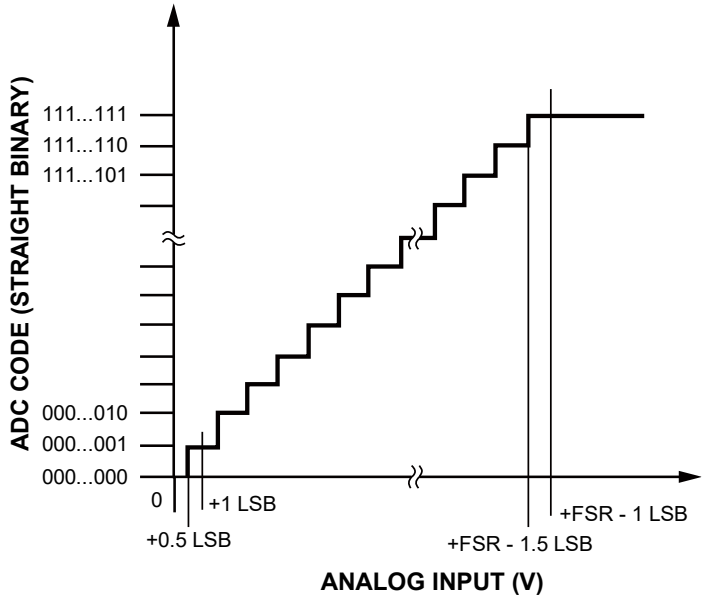


Figure 26. ADC Ideal Transfer Function of Singled-ended or Pseudo Differential Unipolar

Singled-ended or Pseudo Differential Unipolar Output Codes and Ideal Input Voltages

Description	Analog Input V_{REF} = 5 V	Digital Output (Hex)
FSR – 1 LSB	4.999981 V	0x3FFFF [1]
Midscale + 1 LSB	2.500019 V	0x20001
Midscale	2.5 V	0x20000
Midscale – 1 LSB	2.499981 V	0x1FFFF
-FSR + 1 LSB	19 µV	0x00001
-FSR	0 V	0x00000 [2]

When configured as pseudo differential bipolar (COM = V_{REF} / 2 or INx- = V_{REF} / 2), the code is twos complement.

1 This is also the code for an overranged analog input ((INx+) – (INx-), above V_{REF} – GND).
2 This is also the code for an underranged analog input ((INx+) – (INx-), below GND).

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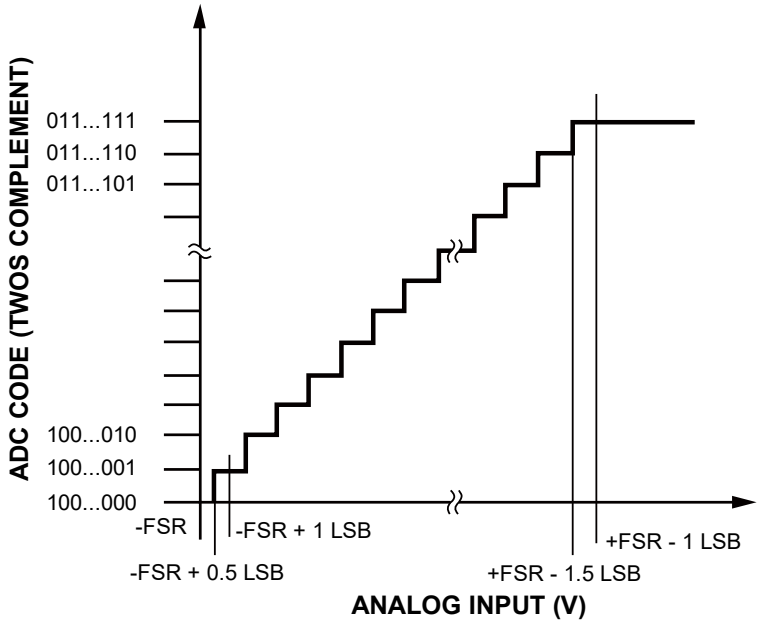


Figure 27. ADC Ideal Transfer Function of Pseudo Differential Bipolar

Pseudo Differential Bipolar Output Codes and Ideal Input Voltages

Description	Analog Input V_{REF} = 5 V	Digital Output (Hex)
FSR – 1 LSB	+2.499981 V	0x1FFFF[1]
Midscale + 1 LSB	+19 µV	0x00001
Midscale	0 V	0x00000
Midscale – 1 LSB	-19 µV	0x3FFFF
-FSR + 1 LSB	-2.499981 V	0x20001
-FSR	-2.5 V	0x20000[2]

1 This is also the code for an overranged analog input ((INx+) – (INx-), above V_{REF} – GND).
2 This is also the code for an underranged analog input ((INx+) – (INx-), below GND).

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Typical Connection

Figure 28 is a suggested connection for the ZJC2103/5-18 when multiple power supplies are used.

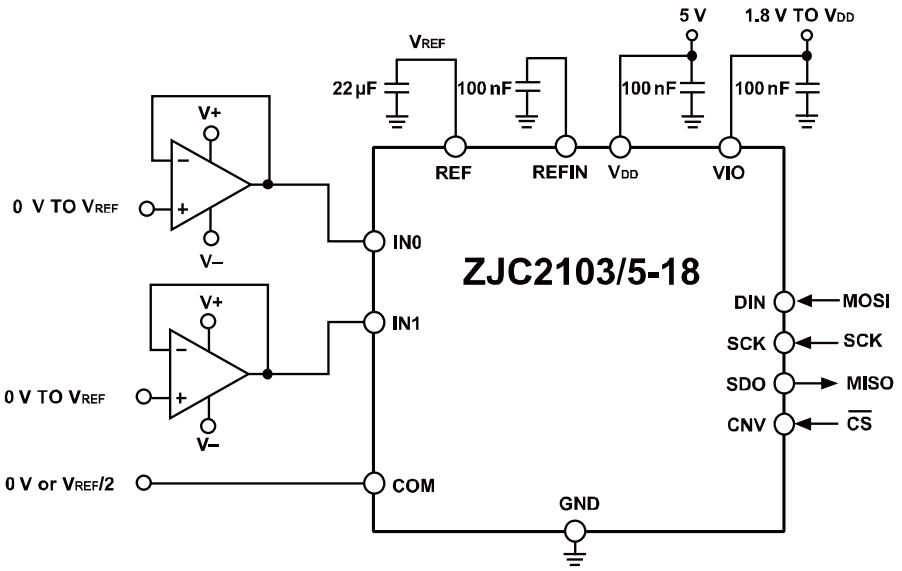


Figure 28. Application Circuits Using Multiple Power Supplies

Figure 29 shows the equivalent circuit of the ZJC2103/5-18 input structure.

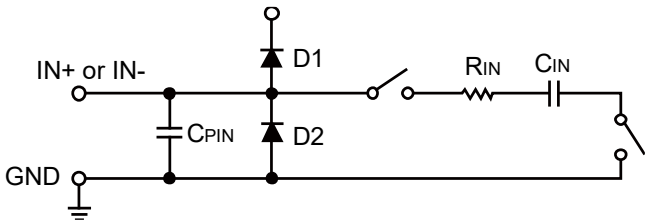


Figure 29. Two Diodes D1 and D2 Provide ESD Protection for the Analog Inputs

The voltage of the analog input signal cannot be higher than the supply voltage (V_{DD}) by more than 0.3 V. If the voltage of the analog input signal exceeds V_{DD} + 0.3 V, the diode will be forward biased and start conducting current. These two diodes can handle forward bias currents up to 50 mA. If the supply voltage of the input driver is higher than V_{DD} the voltage of the analog input signal may be more than 0.3 V higher than the supply voltage. The two diodes D1 and D2 provide ESD protection for analog input IN+ and IN-.

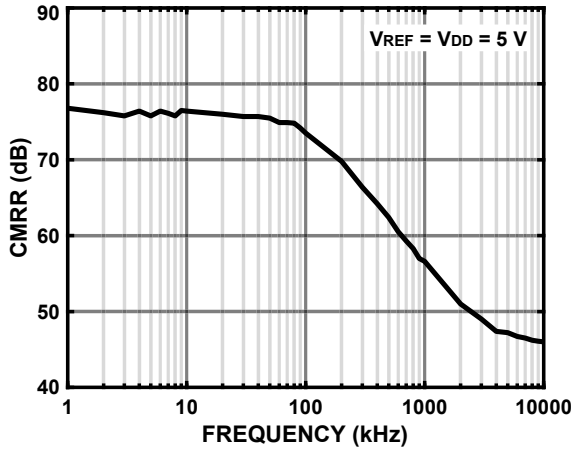


Figure 30. Analog Input CMRR vs. Frequency

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In the acquisition phase, the impedance of the analog inputs can be modeled as a parallel combination of the capacitor, C_{PIN}, and the network formed by the series connection of R_{IN} and C_{IN}. C_{PIN} is primarily the pin capacitance. R_{IN} is typically 700 Ω and is a lumped component composed of serial resistors and the on resistance of the switches. C_{IN} is typically 30 pF and is mainly the ADC sampling capacitor.

Fully Differential to Single-ended Driver

For applications using fully differential analog signals (bipolar or unipolar), an op amp driver can provide pseudo differential unipolar input to the ZJC2103/5-18, see Figure 31 for the schematic diagram.

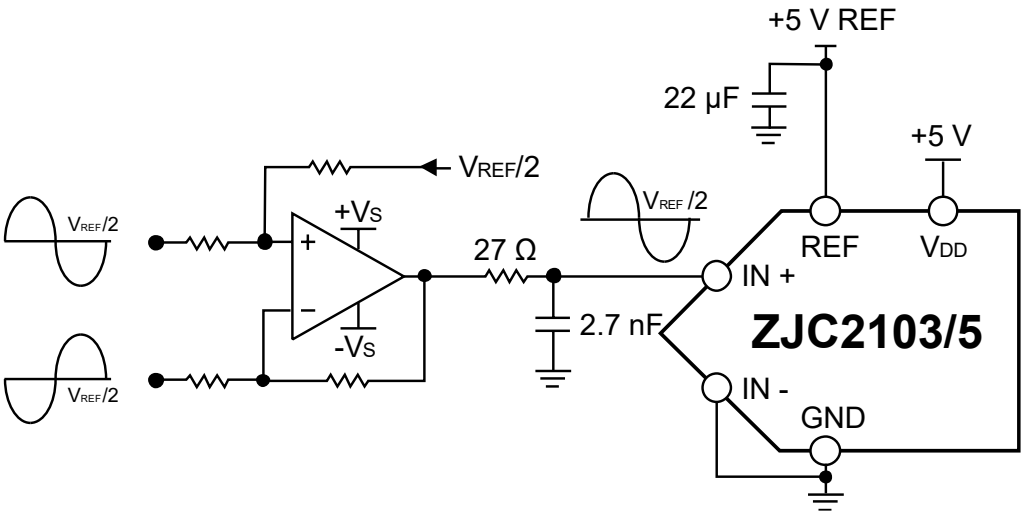


Figure 31. Fully Differential to Single-ended Conversion with an Op Amp

Singled-ended bipolar signal can be converted to pseudo differential unipolar signal with two amplifiers for ZJC2103/5-18.

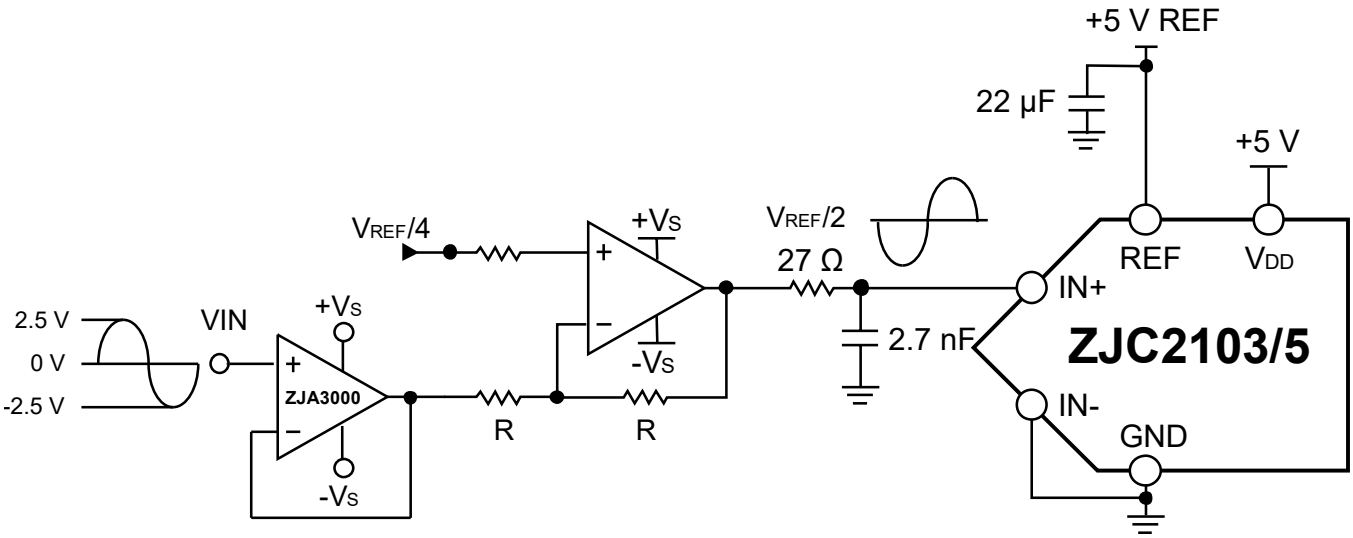


Figure 32. Single-ended Bipolar to Pseudo Differential Unipolar

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Input Configurations

Figure 33 shows configuring the analog inputs with the configuration register CFG [12 : 10].

The analog inputs can be configured as:

- Figure 33A, all single-ended INx inputs referenced to ground; CFG [12 : 10] = 111. In this configuration, all inputs (IN [7 : 0]) have a range of GND to V_{REF}.
- Figure 33B, pseudo differential bipolar with a common reference point; COM = V_{REF} / 2; CFG [12 : 10] = 010. Pseudo differential unipolar with COM = 0 V; CFG [12 : 10] = 110. All inputs IN [7 : 0] referred to GND have a range of GND to V_{REF}.
- Figure 33C, pseudo differential bipolar pairs with the negative input channel referenced to V_{REF}/2; CFG [12 : 10] = 00X. Pseudo differential unipolar pairs with the negative input channel referenced to a ground sense; CFG [12 : 10] = 10X. In these configurations, the positive input channels have the range of GND to V_{REF}. The negative input channels are senses referred to V_{REF}/2 for bipolar pairs, or GND for unipolar pairs. If CFG [9 : 7] is even, then IN0, IN2, IN4, and IN6 are used as positive inputs. If CFG [9 : 7] is odd, then IN1, IN3, IN5, and IN7 are used as positive inputs. Note that for the sequencer, the positive channels are always IN0, IN2, IN4, and IN6.
- Figure 33D, inputs configured in any of the combinations above.

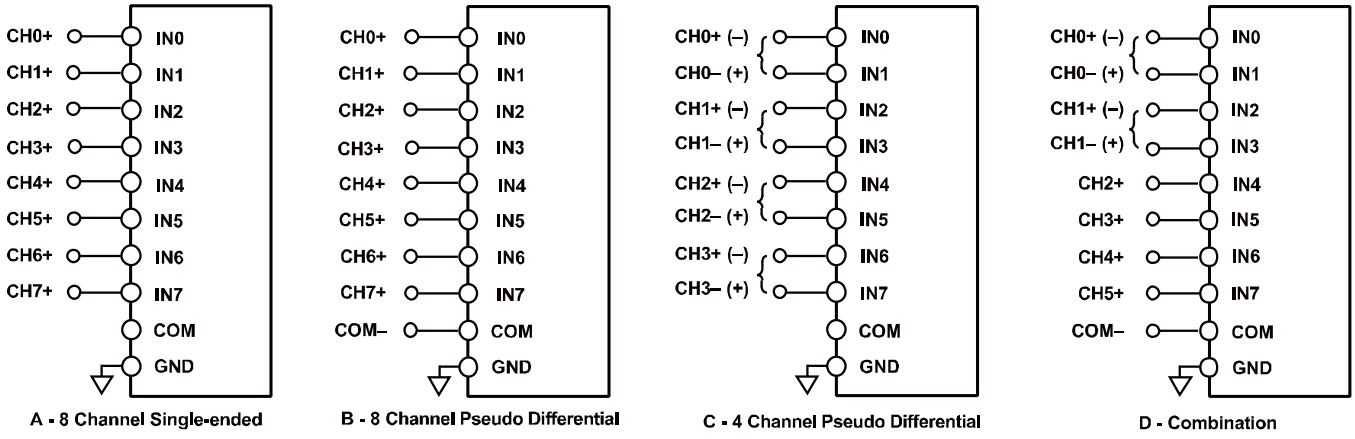


Figure 33. Multiplexed Analog Input Configurations

Internal Reference/Temperature

The ZJC2103/5-18 internal precision reference, can be set for either a 2.5 V or a 4.096 V on REF pin. When the internal reference is enabled, the band gap voltage is present on the REFIN pin. Because the current output of REFIN is limited, it can be used as a source if followed by a suitable buffer, such as the ZJA3000. Note that the voltage of REFIN changes depending on the 2.5 V or 4.096 V internal reference.

Enabling the reference also enables the internal temperature sensor, which measures the internal temperature of the ZJC2103/5-18. Note that, when using the temperature sensor, the output is straight binary referenced ZJC2103/5-18 GND pin.

The internal reference is trimmed to provide a typical drift of ±6 ppm/°C. Figure 34 shows the internal reference connection.

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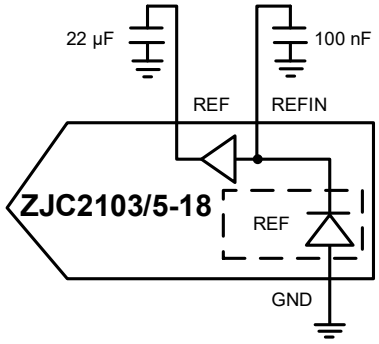


Figure 34. 2.5 V or 4.096 V Internal Reference Connection

External Reference and Internal Buffer

For improved drift performance, an external reference can be used with the internal buffer, as shown in Figure 35. The external source is connected to REFIN, the input to the on-chip unity gain buffer, and the output is produced on the REF pin to drive the ADC core. An external reference can be used with the internal buffer with or without the temperature sensor enabled.

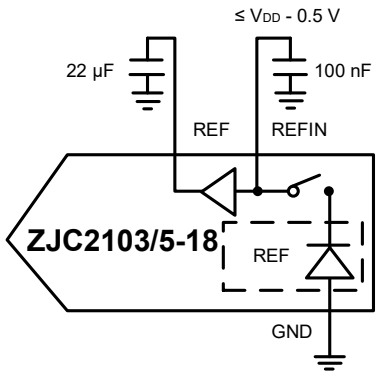


Figure 35. External Reference Using Internal Buffer

External Reference

For improved drift or noise performance, an external reference can be connected directly on the REF pin as shown in Figure 36. The reference buffer must be powered down, and the internal reference can be disabled for lower power consumption.

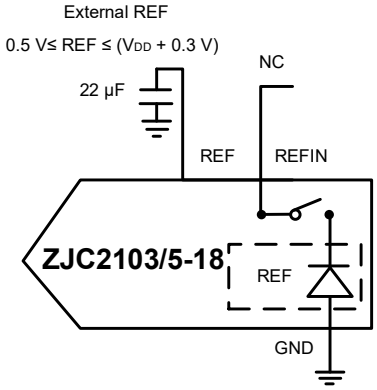


Figure 36. External Reference (internal buffer disabled)

For precision ADC applications, a precision voltage reference is an essential device. Generally, the reference source needs to have low initial error, low noise, and low temperature drift. The ZJC2103/5-18 reference voltage REF has a dynamic input impedance, so it

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should be driven with a low impedance source. The REF and GND pins should be effectively decoupled as described in the PCB Layout Guidelines section. Figure 37 shows an example of a specific voltage reference and driver design. The ZJR100X series of high-precision voltage references can just meet these requirements.

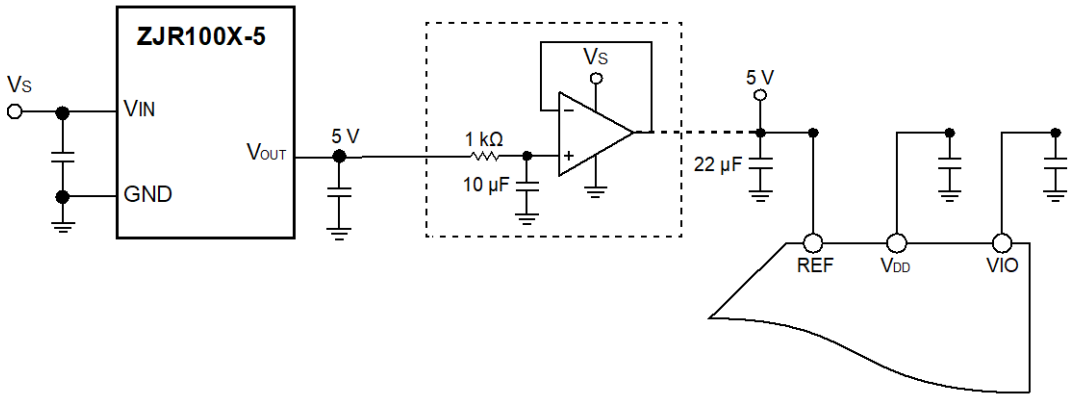


Figure 37. External Reference Drive

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Power Supply

ZJC2103/5-18 uses two power supply pins: core power supply (V_{DD}) and digital input/output interface power supply VIO. VIO can directly interface with any logic from 1.8 V to V_{DD}. To reduce the number of power supplies required, the VIO and V_{DD} pins can be tied together via resistors or ferrite beads. The PSRR curve is shown in Figure 38.

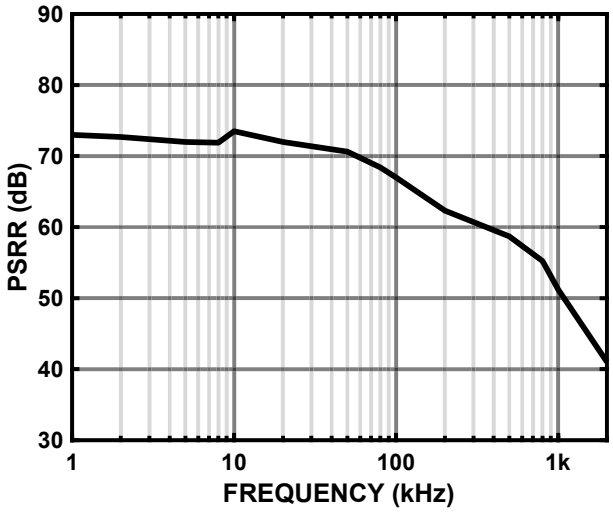


Figure 38. PSRR vs. Frequency

The ZJC2103/5-18 automatically enters power-down mode at the end of each conversion stage, so the power consumption is approximately linearly proportional to the sampling rate. This makes the device suitable for low sampling rate and low power consumption applications. As shown Figure 39.

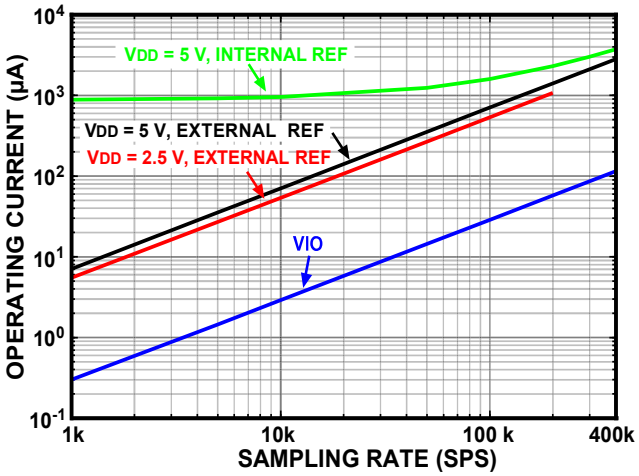


Figure 39. Operating Current vs. Sampling Rate

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Digital Interface

ZJC2103/5-18 has 4-wire SPI digital interface which uses CNV, DIN, SCK and SDO. A 14-bit register, CFG [13 : 0], is used to configure the ADC for the channel to be converted, the reference selection, and other components.

When CNV is low (works like chip select), reading/writing can occur during conversion, acquisition, and spanning conversion (acquisition plus conversion), as detailed in the following sections. The CFG word is updated on the first 14 SCK rising edges, and conversion codes are output on the first 17 (or 18 if busy indicator is selected) SCK falling edges. If the CFG readback is enabled, an additional 14 SCK falling edges are required to output the CFG word following the conversion code with the CFG MSB following the LSB of the conversion code.

Reading/Writing During Conversion

When reading or writing during conversion (n), conversion results are for the previous (n - 1) conversion, and writing the CFG register is for the next (n + 1) acquisition and conversion. After the CNV is brought high to initiate conversion, it must be brought low again to allow reading or writing during conversion. Reading or writing should only occur up to t_{DATA}.

The SCK frequency required is calculated by

$$f_{SCK} \geq \frac{Number_SCK_Edges}{t_{DATA}}$$

The time between t_{DATA} and t_{CONV} is a quiet time when digital activity should not occur, or sensitive bit decisions may be corrupted.

Reading/Writing After Conversion

When reading or writing after conversion, or during acquisition (n), conversion results are for the previous (n - 1) conversion, and writing is for the (n + 1) acquisition. The reading or writing takes place during the t_{ACQ} (minimum) time.

Reading/Writing Spanning Conversion

When reading or writing spanning conversion, the data access starts at the current acquisition (n) and spans into the conversion (n). Conversion results are for the previous (n - 1) conversion, and writing the CFG register is for the next (n + 1) acquisition and conversion.

Configuration Register

The ZJC2103/5-18 uses a 14-bit configuration register (CFG [13 : 0]) to configure the analog inputs, the channel to be converted, the one-pole filter bandwidth, the reference, and the channel sequencer. The CFG register is latched (MSB first) on DIN with 14 SCK rising edges.

The register can be written to during conversion, during acquisition, or spanning acquisition/conversion, and is updated at the end of conversion. There is always a one deep delay when writing the CFG register. Note that, at power-up, the CFG register is undefined and two dummy conversions are required to update the register. To preload the CFG register with a factory setting, hold DIN high for two conversions. Thus CFG [13 : 0] = 0b11 1111 1111 1111. This sets the ZJC2103/5-18 for the following:

- IN [7 : 0] unipolar referenced to GND, sequenced in order
- Full bandwidth
- Internal reference and temperature sensor disabled, buffer enabled
- Internal sequencer enabled
- No readback of the CFG register

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13	12	11	10	9	8	7	6	5	4	3	2	1	0
CFG	INCC	INCC	INCC	INX	INX	INX	BW	REF	REF	REF	SEQ	SEQ	RB

Configuration Register Description:

Bit	Name	Description
[13]	CFG	Configuration update. 0 = write invalid, keep current configuration settings. 1 = write enabled, overwrite contents of register.
[12 : 10]	INCC	Input channel configuration. Selection of pseudo differential bipolar, pseudo differential unipolar pairs, single-ended, or temperature sensor.

12	11	10	Function
0	0	X[1]	Pseudo differential bipolar pairs; INx- input is V_{REF} / 2 ± 0.1 V.
0	1	0	Pseudo differential bipolar pairs; INx- is COM = V_{REF} / 2 ± 0.1 V.
0	1	1	Temperature sensor.
1	0	X	Pseudo differential unipolar pairs; INx- input is GND ± 0.1 V.
1	1	0	Pseudo differential unipolar pairs; INx- is COM = GND ± 0.1 V.
1	1	1	Singled-ended; INx referenced to GND.

[9 : 7] INx — Input channel selection.

ZJC2103-18				ZJC2105-18			
9	8	7	Channel selected	9	8	7	Channel selected
0	0	0	IN0	X	0	0	IN0
0	0	1	IN1	X	0	1	IN1
…	…	…	…	X	1	0	IN2
1	1	1	IN7	X	1	1	IN3

Bit	Name	Description
[6]	BW	Selection of bandwidth for low-pass filter. 0 = ¼ BW, an additional internal series resistor to limit the noise. Maximum throughput must be reduced to ¼. 1 = Full bandwidth.
[5 : 3]	REF	Reference or buffer selection. Selection of internal, external, external buffered, and enabling of the on-chip temperature sensor.

5	4	3	Function
0	0	0	Internal reference and temperature sensor enabled. REF = 2.5 V buffered output.
0	0	1	Internal reference and temperature sensor enabled. REF = 4.096 V buffered output.
0	1	0	Use external reference on REF. Temperature sensor enabled. Internal buffer disabled.
0	1	1	Use external reference on REFIN. Temperature sensor enabled. Internal buffer enabled.
1	0	0	Invalid.
1	0	1	Invalid.
1	1	0	Use external reference on REF. Temperature sensor disable, internal reference disabled and internal buffer disabled.
1	1	1	Use external reference on REFIN. Temperature sensor disable, internal reference disabled and internal buffer enabled.

[2 : 1] SEQ — Channel sequencer. Allows for scanning channels in an IN0 to IN [7 : 0] fashion.

2	1	Function
0	0	Disable sequencer.
0	1	No effect.
1	0	Scan IN0 to IN [7 : 0] (set in CFG [9 : 7]), then temperature.
1	1	Scan IN0 to IN [7 : 0] (set in CFG [9 : 7])

Bit	Name	Description
[0]	RB	Read back the CFG register. 0 = Read back current configuration at end of code. 1 = Do not read back current configuration at end of code.

[1] X = do not care

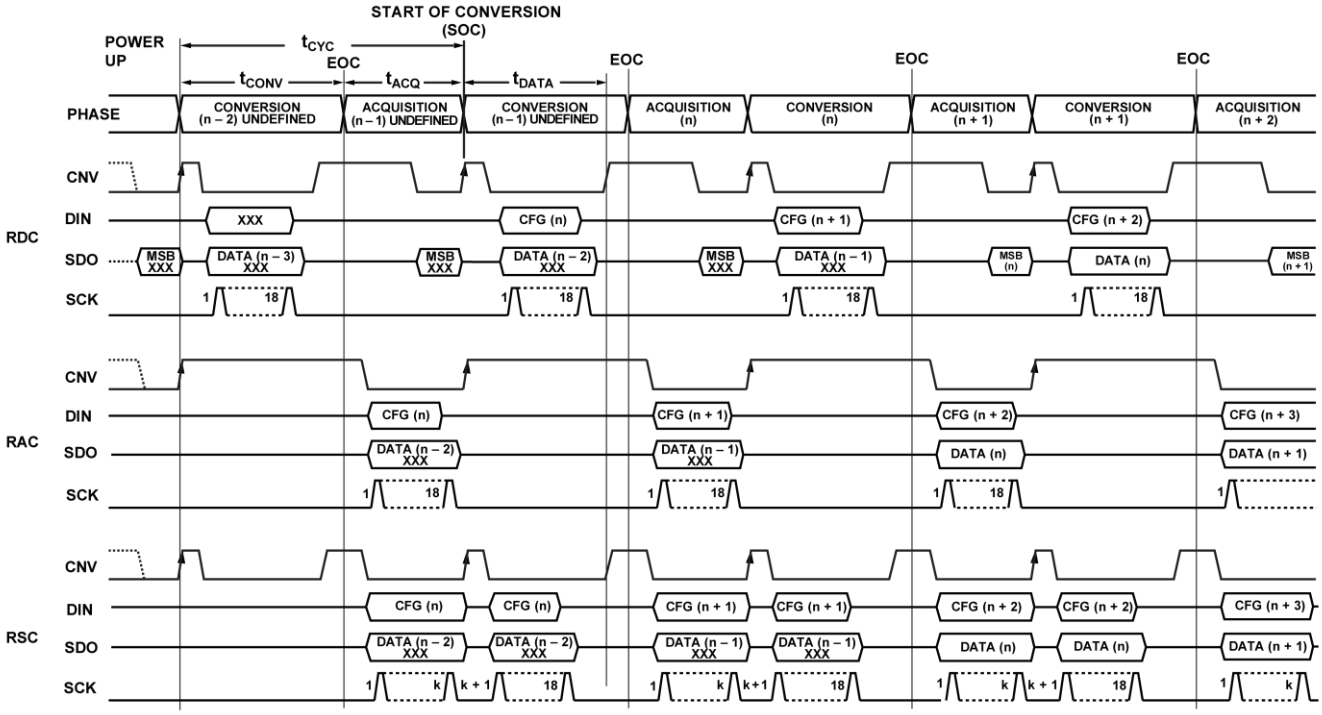
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General Timing Without a Busy Indicator

Figure 40 details the timing for all three modes: read/write during conversion (RDC), read/write after conversion (RAC), and read/write spanning conversion (RSC). Note that the gating item for both CFG and code readback is at the end of conversion (EOC). Make sure CNV is high at EOC, so the busy indicator is disabled.

The data access should happen during the safe data reading/writing time, t_{DATA}. If the full CFG word was not written to before EOC, it is discarded and the current configuration remains. If the conversion result is not read out fully prior to EOC, it is lost as the ADC updates SDO with the MSB of the current conversion. When CNV is brought low after EOC, SDO is driven from high impedance to the MSB. Falling SCK edges clock out bits starting with MSB -1. The SCK can idle high or low.

From power-up, in any read/write mode, the first three conversion results are undefined because a valid CFG does not take place until the 2nd EOC; thus two dummy conversions are required. Also, if the state machine writes the CFG during the power-up state (RDC shown), the CFG register needs to be rewritten again at the next phase. Note that the first valid data occurs in Phase (n + 1) when the CFG register is written during Phase (n - 1).



Note: n = 18 for no readback of CFG; n = 32 for readback of CFG

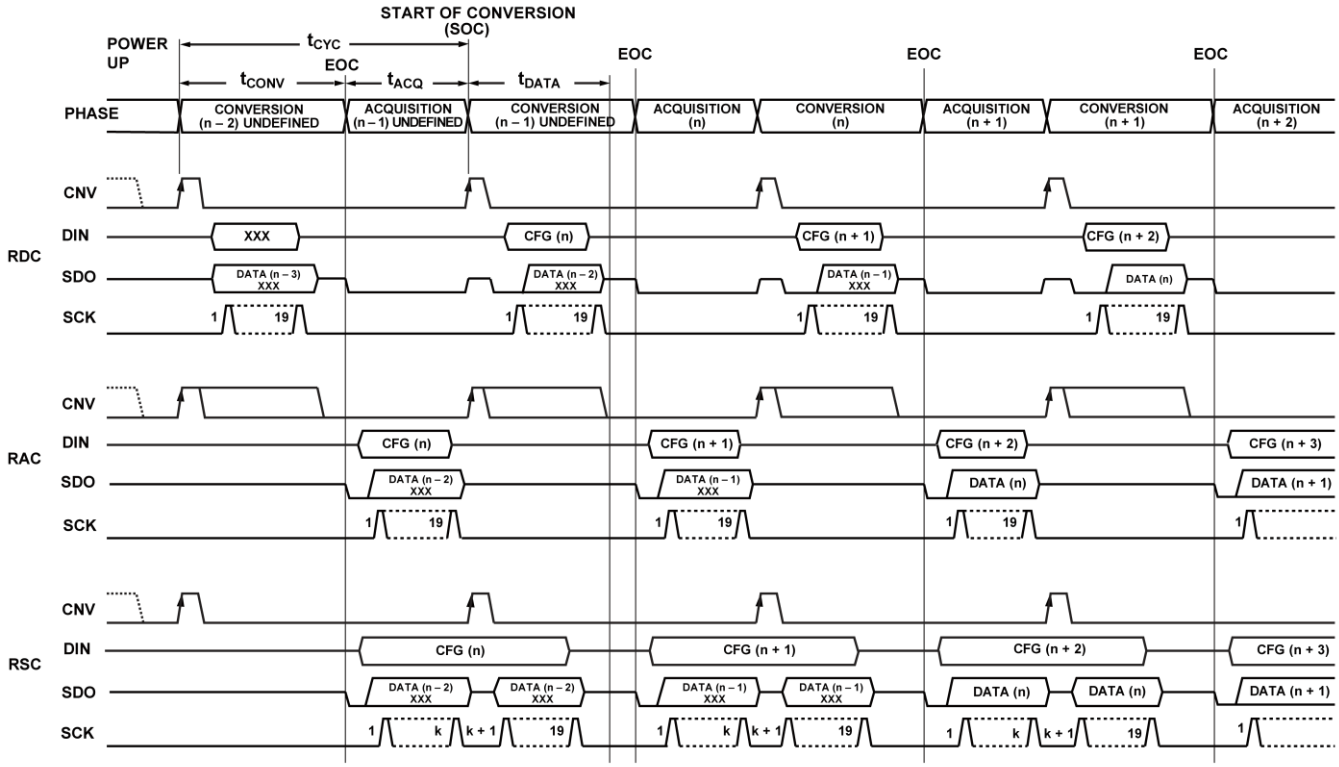
Figure 40. General Interface Timing for the ZJC2103/5-18 Without a Busy Indicator

General Timing with a Busy Indicator

Figure 41 details the timing for all three modes: read/write during conversion (RDC), read/write after conversion (RAC), and read/write spanning conversion (RSC). If CNV is low at EOC, the busy indicator is enabled. In addition, to generate the busy indicator properly, the host must provide a minimum of 17 SCK falling edges to return SDO to high impedance because the last bit on SDO remains active.

From power-up, in any read/write mode, the first three conversion results are undefined because a valid CFG does not take place until the 2nd EOC; thus two dummy conversions are required. If the host writes the CFG during the power-up state (RDC shown), the CFG register needs to be rewritten again at the next phase. Note that the first valid data occurs in Phase (n + 1) when the CFG register is written during Phase (n - 1).

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Note: n = 19 for no readback of CFG; n = 33 for readback of CFG

Figure 41. General Interface Timing for the ZJC2103/5-18 With a Busy Indicator

Channel Sequencer

ZJC2103/5-18 channels can be scanned as singles or pairs, with or without the temperature sensor.

The sequencer starts with IN0 and ends with IN [7 : 0] set in CFG [9 : 7]. For paired channels, the channels are paired depending on the last channel set in CFG [9 : 7]. Note that in sequencer mode, the channels are always paired with the positive input on the even channels (IN0, IN2, IN4, IN6), and with the negative input on the odd channels (IN1, IN3, IN5, IN7).

Figure 42 shows the timing for all three modes without a busy indicator. The sequencer can also be used with the busy indicator.

For sequencer operation, the CFG register should be set during the (n - 1) phase. On phase (n), the sequencer setting takes place and acquires IN0. The first valid conversion code is available at phase (n + 1). After the last channel set in CFG [9 : 7] is converted, the internal temperature sensor data is output (if enabled), followed by acquisition of IN0.

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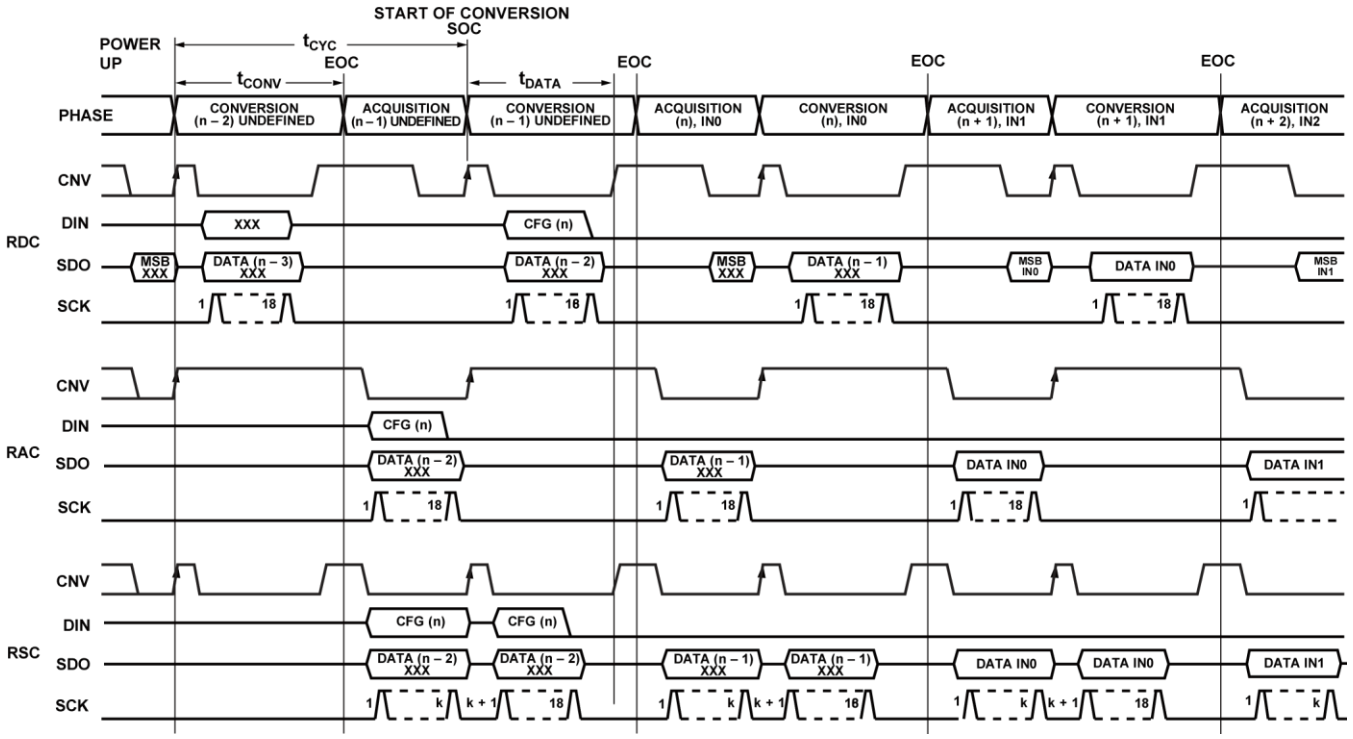


Figure 42. General Channel Sequencer Timing Without a Busy Indicator

RAC Without a Busy Indicator

ZJC2103/5-18 connects to the host as shown in Figure 43, and the timing is shown is Figure 44.

A rising edge on CNV initiates a conversion, pushes SDO to high impedance, and ignores data present on DIN. After a conversion is initiated, it continues until completion independent of the state of CNV. CNV must be returned high before the t_{DATA} elapses, and then held high beyond the conversion time t_{CONV}, to avoid the busy indicator generation.

After the conversion is complete, the ZJC2103/5-18 enters the acquisition phase and powers down. While CNV is low, both a CFG update and a data readback take place. The first 14 SCK rising edges are used to update the CFG, and the first 17 SCK falling edges clock out the conversion results starting with MSB - 1. All 14 bits of CFG [13 : 0] must be written, otherwise they are ignored.

After the 18th (or 32th) SCK falling edge, or when CNV goes high (whichever happens first), SDO returns to high impedance.

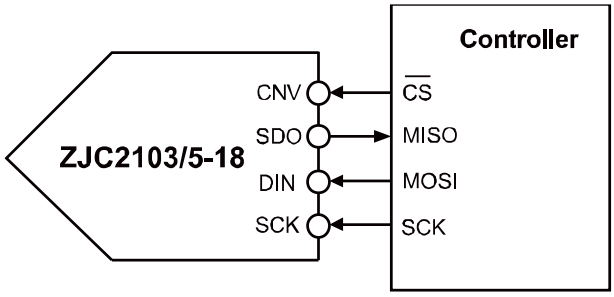


Figure 43. Connection without a Busy Indicator

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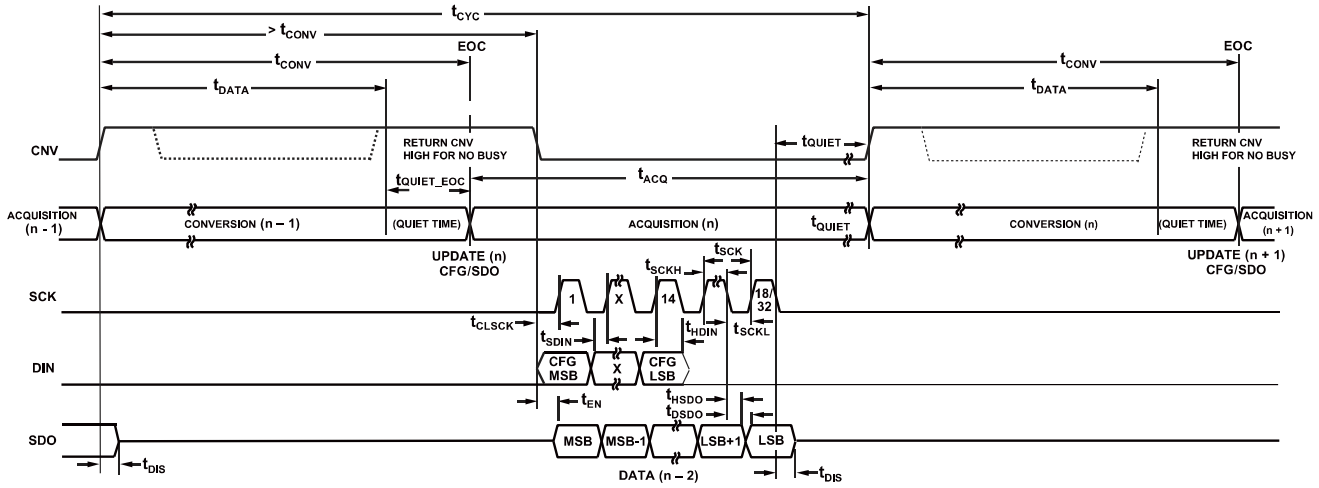


Figure 44. Timing of RAC without a Busy Indicator

RAC with a Busy Indicator

ZJC2103/5-18 connects to the host as shown in Figure 45, and the timing is shown is Figure 46.

A rising edge on CNV initiates a conversion, pushes SDO to high impedance, and ignores data present on DIN. After a conversion is initiated, it continues until completion independent of the state of CNV. CNV must be returned low before the t_{DATA} elapses, and then held low beyond the conversion time t_{CONV}, to generate the busy indicator.

After the conversion is complete, the ZJC2103/5-18 enters the acquisition phase and powers down. While CNV is low, both a CFG update and a data readback take place. The first 14 SCK rising edges are used to update the CFG, and the first 18 SCK falling edges clock out the conversion results. All 14 bits of CFG [13 : 0] must be written, otherwise they are ignored.

After the 18th (or 32th) SCK falling edge, or when CNV goes high (whichever happens first), SDO returns to high impedance.

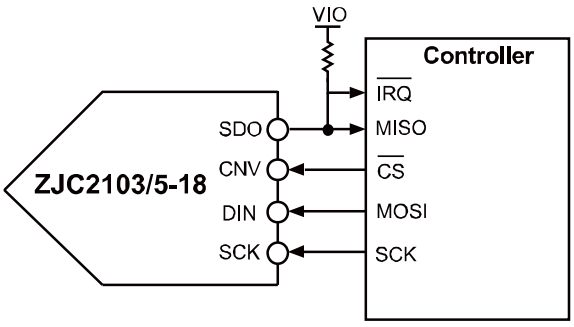


Figure 45. Connection with a Busy Indicator

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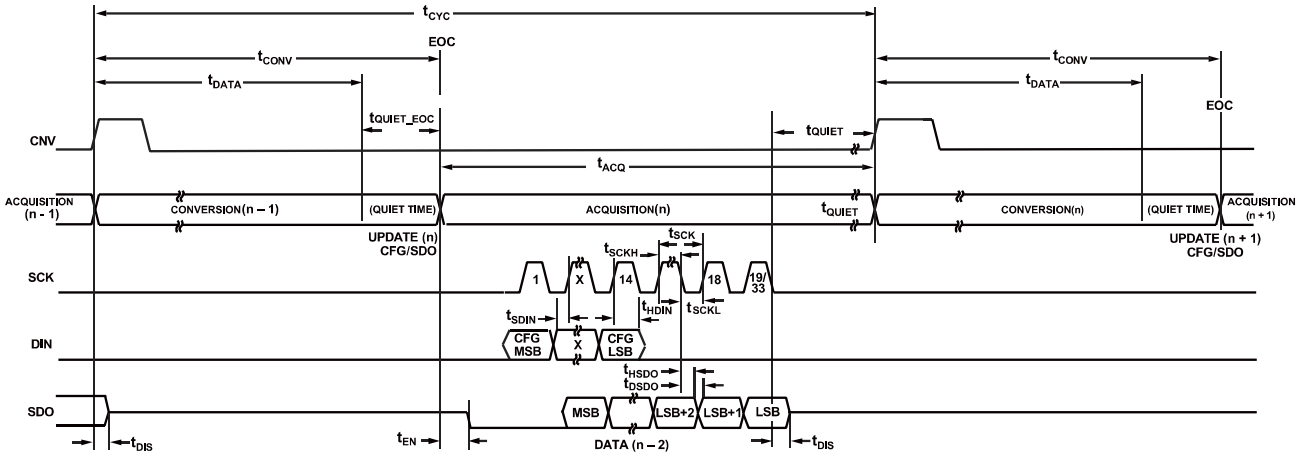


Figure 46. Timing of RAC with a Busy Indicator

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Layout Guidelines

For optimum performance of the device, good PCB layout practices are recommended, including:

- Avoid running digital lines under the device, which may couple noise onto the die, unless a ground plane under the ZJC2103/5-18 is used as a shield. Fast switching signals such as CNV or clocks should not be placed close to the analog signal path. Crossover of digital and analog signals should be avoided.
- At least one ground plane should be used. It can be common or split between the digital and analog sections. In the latter case, the planes should be joined close to the ZJC2103/5-18.
- The ZJC2103/5-18 external voltage reference input, REF, has a dynamic input impedance and should be decoupled with 10 or 22 µF ceramic capacitors to minimize parasitic inductances. This is done by placing the reference decoupling ceramic capacitor close to, ideally right up against, the REF and GND pins and connecting them with wide, low impedance trace.
- The power supply V_{DD} of ZJC2103/5-18 should be decoupled with 10 µF and 100 nF ceramic capacitors, placed close to the ZJC2103/5-18 and connected using short, wide traces to provide low impedance paths and to reduce the effect of noises on the power supply lines.

Figure 47 is an example of the guidance.

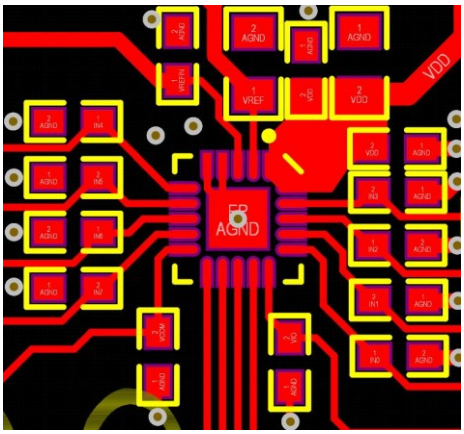


Figure 47. Example Layout and Routing of ZJC2103/5-18

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Outline Dimensions

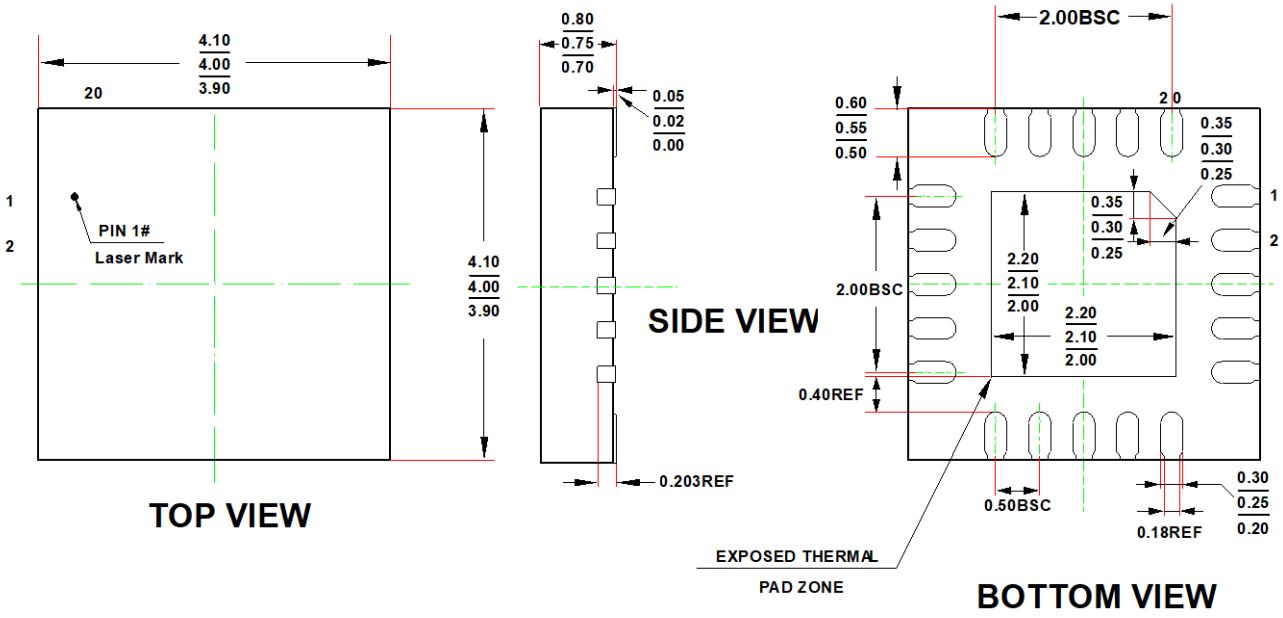


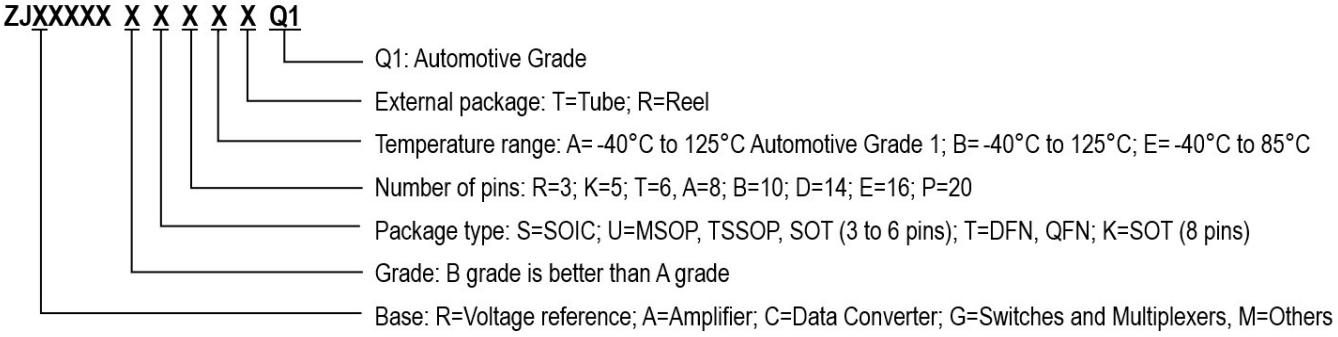
Figure 48. 20-Lead QFN Package Dimensions Shown in Millimeter

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Ordering Guide

Model	Orderable Device	Status [1]	Resolution (bit)	Supply Voltage (V)	Temperature Range (°C)	Package	External Package
ZJC2103-18	ZJC2103-18ATPER	ACTIVE	18	2.3 to 5.5	-40 to +85	QFN-20	13" Reel
ZJC2105-18	ZJC2105-18ATPER	ACTIVE					

Product Order Model



[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: ZJW has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but ZJW does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may be available.
OBSOLETE: ZJW has discontinued the production of the device.

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Related Parts

Part Number	Description	Comments
ADC		
ZJC2020	20-bit 350 kSPS SAR ADC	Fully differential input, SINAD 101.4 dB, THD -118 dB
ZJC2000/2010	18-bit 400 kSPS/200 kSPS SAR ADC	Fully differential input, SINAD 99.3 dB, THD -113 dB
ZJC2001/2011	16-bit 500 kSPS/250 kSPS SAR ADC	Fully differential input, SINAD 95.3 dB, THD -113 dB
ZJC2002/2012 ZJC2003/2013	16-bit 500 kSPS/250 kSPS SAR ADC	Pseudo-differential unipolar input, SINAD 91.7 dB, THD -105 dB Pseudo-differential bipolar input, SINAD 91.7 dB, THD -105 dB
ZJC2004/2014 ZJC2005/2015	18-bit 400 kSPS/200 kSPS SAR ADC	Pseudo-differential unipolar input, SINAD 94.2 dB, THD -105 dB Pseudo-differential bipolar input, SINAD 94.2 dB, THD -105 dB
ZJC2007/2017 ZJC2008/2018	14-bit 600 kSPS/300 kSPS SAR ADC	Pseudo-differential unipolar input, SINAD 85 dB, THD -105 dB Pseudo-differential bipolar input, SINAD 85 dB, THD -105 dB
ZJC2009	Small size, 12-bit 1 MSPS SAR ADC	Single-ended input, SOT23-6, 2.3 V to 5 V, SINAD 73 dB, THD -89 dB
ZJC2100/1-18 ZJC2100/1-16	18-bit 400 kSPS/200 kSPS 4-ch differential SAR ADC, SINAD 99.3 dB, THD -113 dB 16-bit 500 kSPS/250 kSPS 4-ch differential SAR ADC, SINAD 95.3 dB, THD -113 dB	
ZJC2102/3-18 ZJC2102/3-16 ZJC2102/3-14	18-bit 400 kSPS/200 kSPS 8-ch pseudo-differential SAR ADC, SINAD 94.2 dB, THD -105 dB 16-bit 500 kSPS/250 kSPS 8-ch pseudo-differential SAR ADC, SINAD 91.7 dB, THD -105 dB 14-bit 600 kSPS/300 kSPS 8-ch pseudo-differential SAR ADC, SINAD 85 dB, THD -105 dB	
ZJC2104/5-18 ZJC2104/5-16	18-bit 400 kSPS/200 kSPS 4-ch pseudo-differential SAR ADC, SINAD 94.2 dB, THD -105 dB 16-bit 500 kSPS/250 kSPS 4-ch pseudo-differential SAR ADC, SINAD 91.7 dB, THD -105 dB	
DAC		
ZJC2541-18/16/14 ZJC2543-18/16/14	18/16/14-bit 1 MSPS single channel DAC with unipolar output	Power on reset to 0 V (ZJC2541) or V_{REF}/2 (ZJC2543), 1 nV-S glitch, SOIC-8, MSOP-10/8, DFN-10 packages
ZJC2542-18/16/14 ZJC2544-18/16/14	18/16/14-bit 1 MSPS single channel DAC with bipolar output	Power on reset to 0 V (ZJC2542) or V_{REF}/2 (ZJC2544), 1 nV-S glitch, SOIC-14, TSSOP-16, QFN 16 packages
Amplifier		
ZJA3000-1/2/4 ZJA3001-1/2/4	Single/Dual/Quad 36 V low bias current precision Op Amps	3 MHz, 35 µV max Vos, 0.5 µV/°C max TCVos, 25 pA max Ibias, 1 mA/ch, input to V- (ZJA3000 only), RRO, 4.5 V to 36 V
ZJA3018-2 ZJA3008-2	OVP ±75 V, 36 V, Low Power, High Precision Op Amp 36 V, Low Power, High Precision Op Amp	1.3 MHz, 10 µV max Vos, 0.5 µV/°C max TCVos, 25 pA max Ibias, 0.5 mA/ch, OVP ±75 V (ZJA3018 only), RRO, 4.5 V to 36 V
ZJA3512-2	Dual 36 V 7 MHz precision JFET Op Amps	7 MHz, 35 V/µS, 50 µV max Vos, 1 µV/°C max TCVos, 2 mA/ch, RRO, 9 V to 36 V
ZJA3206/06/02-1/2	Precision 24/11.6/5.3 MHz CMOS RRIO Op Amps	24/11.6/5.3 MHz, RRIO, 30 µV max Vos, 1 µV/°C max TCVos, 0.6 pA Ib, 2.7 V to 5.5 V
ZJA3600/1	36 V ultra-high precision in-amp	CMRR 105 dB min (G = 1), 25 pA max Ib, 25 µV max Vosi, ±2.4 V to ±18 V, -40 °C to 125 °C
ZJA3611, ZJA3609	36 V precision wider bandwidth precision in-amp (G ≥ 10)	CMRR 120 dB min (G = 10), 25 pA max Ibias, 25 µV max Vosi, 1.2 MHz BW (G = 10)
ZJA3676/7 ZJA3678/9	Low power, G = 1 Single/Dual 36 V difference amplifier Low power, G = 0.5/2 Single/Dual 36 V difference amplifier	Input protection to ±65 V, CMRR 104 dB min (G = 1), Vos 100 µV max, gain error 15 ppm max, 500 kHz BW (G = 1), 330 µA/channel, 2.7 V to 36 V
ZJA3669	High Common-Mode Voltage Difference Amplifier	±270 V CMV, 2.5 kV ESD, 96 dB min CMRR, 450 kHz BW, 4 V to 36 V, SOIC-8
ZJA3100	15 V precision fully differential amplifier	145 MHz, 447 V/µS, 50 nS to 16-bit, 50 µV max Vos, 4.6 mA Iq, SOIC/MSOP-8, QFN-16
ZJA3236/26/22-2	Low-cost 22/10/5 MHz CMOS RRIO Op Amps	22/11/5 MHz, RRIO, 2 mV max Vos, 6 µV/°C max TCVos, 0.6 pA Ib, 2.7 V to 5.5 V
ZJA3622/8	36 V low-cost precision in-amp	0.5 nA max Ibias, 125 µV max Vosi, 625 kHz BW (G = 10), 3.3 mA Iq, ±2.4 V to ±18 V
Voltage Reference		
ZJR1004	40 V supply precision voltage reference	V_{OUT} = 2.048/2.5/3/3.3/4.096/5/10 V, 5 ppm/°C max drift -40 °C to 125 °C
ZJR1001/2 ZJR1003	5.5 V low power voltage reference (ZJR1001 with noise filter option)	V_{OUT} = 2.048/2.5/3/3.3/4.096/5 V, 5 ppm/°C max drift -40 °C to 125 °C, ±0.05% initial error, 130 µA, ZJR1001/2 in SOT23-6, ZJR1003 in SOIC/MSOP-8
ZJR1302	5.5 V low power compact precision voltage reference	V_{OUT} = 2.048/2.5/3/3.3/4.096 V, 30 ppm/°C max drift -40 °C to 125 °C, 130 µA, SOT23-3
Switches and Multiplexers		
ZJG4438/4439	36 V fault protection 8:1/dual 4:1 multiplexer	Protection to ±50 V power on & off, latch-up immune, Ron 270 Ω, 14.8 pC, t_{ON} 166 nS
ZJG4428/4429	36 V 8:1/dual 4:1 multiplexer	Latch-up immune, Ron 270 Ω, 14.8 pC charge injection, t_{ON} 166 nS
Quad Matching Resistor		
ZJM5400	±75 V precision match resistors	Mismatch < 100 ppm, 10k:10k:10k:10k, 100k:100k:100k:100k, 100k:10k:10k:100k, 1k:1k:1k:1k, 1M:1M:1M:1M, 5k:1k:1k:5k, 5k:1.25k:1.25k:5k, 9k:1k:1k:9k, ESD: 3.5 kV

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